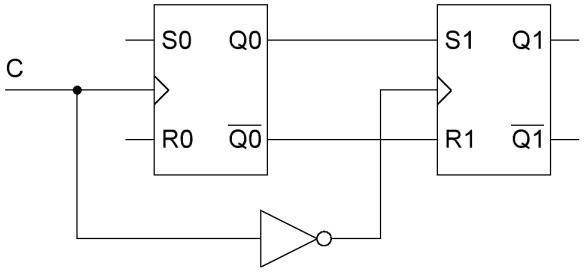
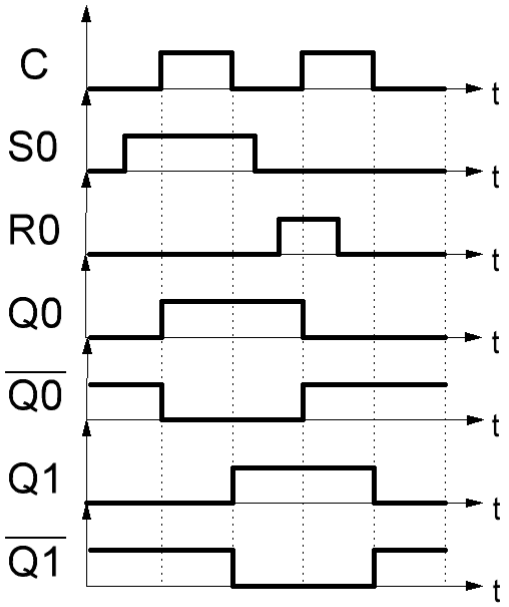
Key to Tutorial 1
Flip-Flops

Exercise 1: RS Flip-Flops

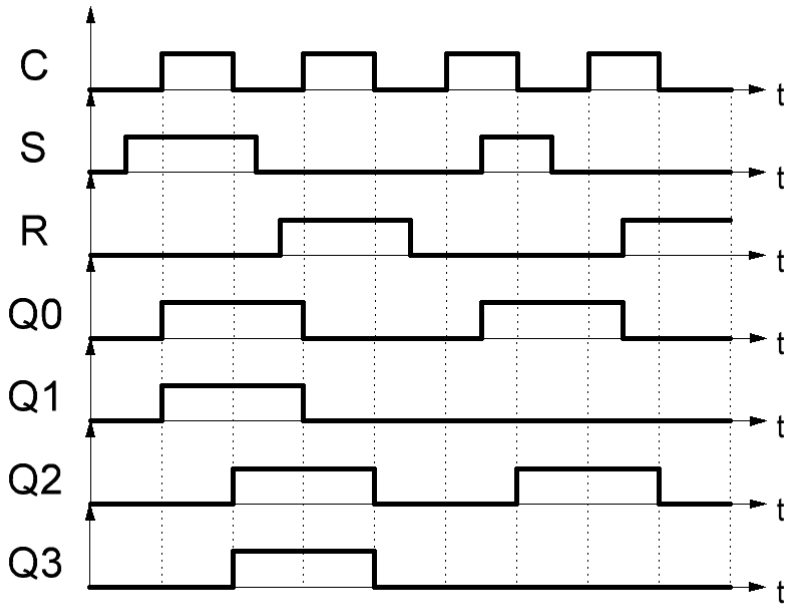
1. Complete the timing diagram for the circuit below. If we consider the whole circuit as only one RS flip-flop, in what way is this flip-flop clocked?



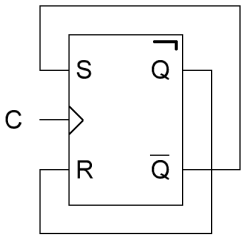
This circuit is a master-slave RS flip-flop.

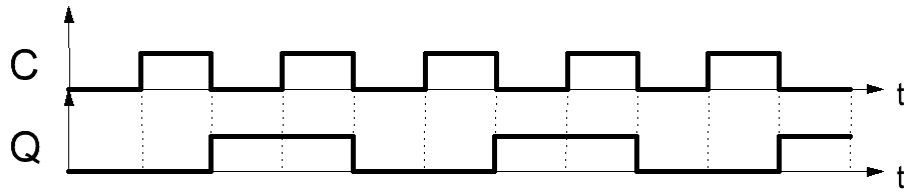


2. Complete the following timing diagrams for a gated RS latch (*Q0*), a positive-edge-triggered RS flip-flop (*Q1*), a negative-edge-triggered RS flip-flop (*Q2*) and a master-slave RS flip-flop (*Q3*).

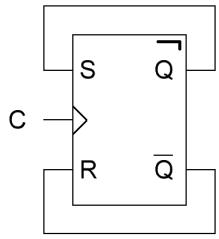


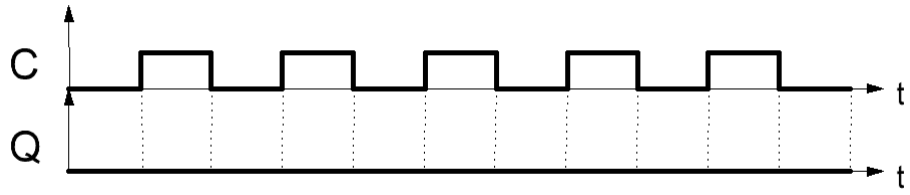
3. Draw the timing diagram of the *Q* output for each of the two circuits below. What is the frequency ratio between *C* and the *Q* output of the first circuit? What is this circuit called?



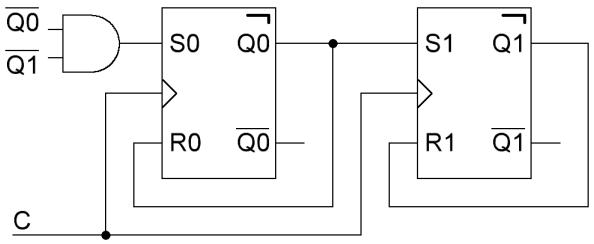


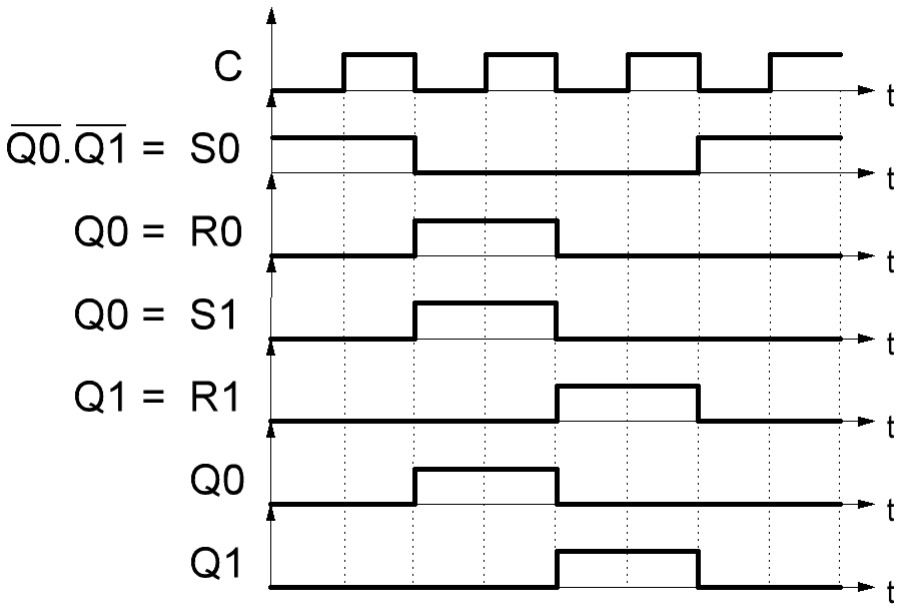
$f_Q/f_C = ½ \rightarrow$ Divide-by-two circuit

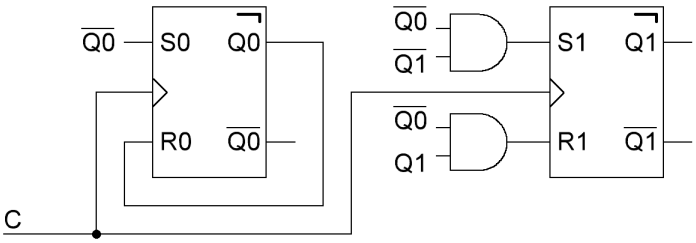


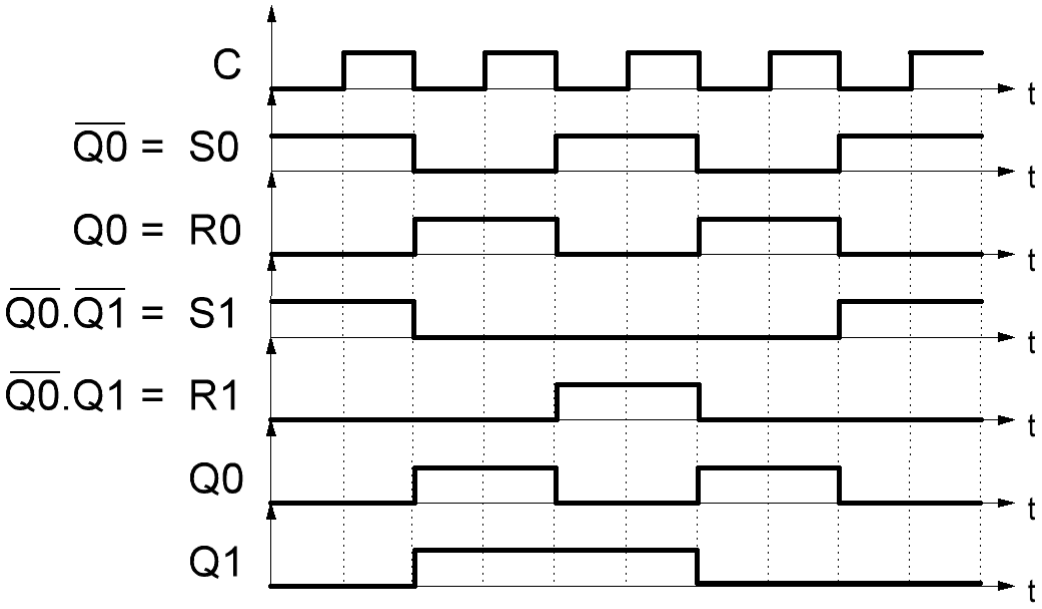


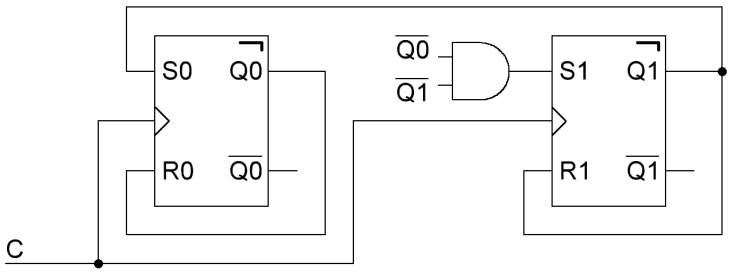
4. Complete the timing diagrams for the circuits below.

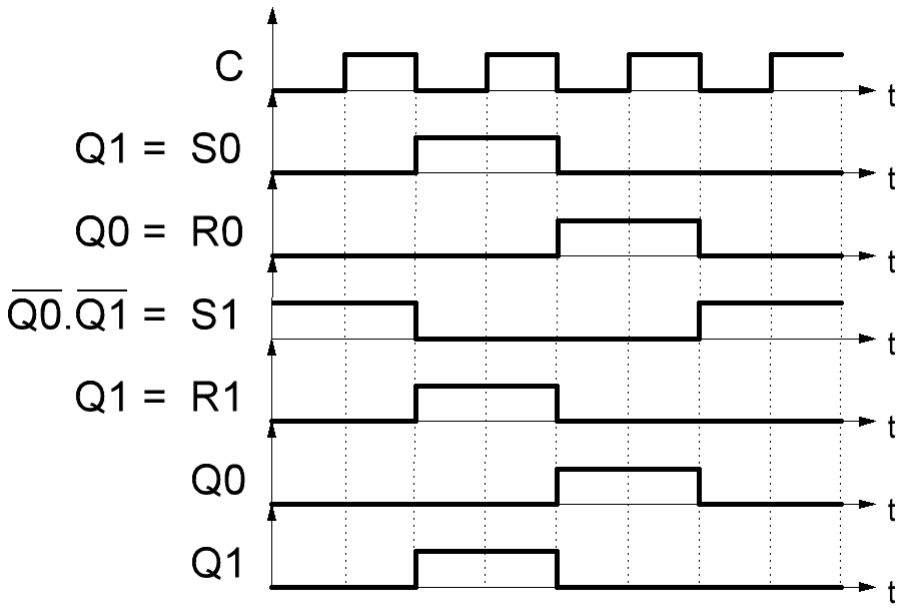





Q0
S0
Q0
R0
Q0
C
Q0
Q1
S1
Q1
Q0
Q1
R1
Q1

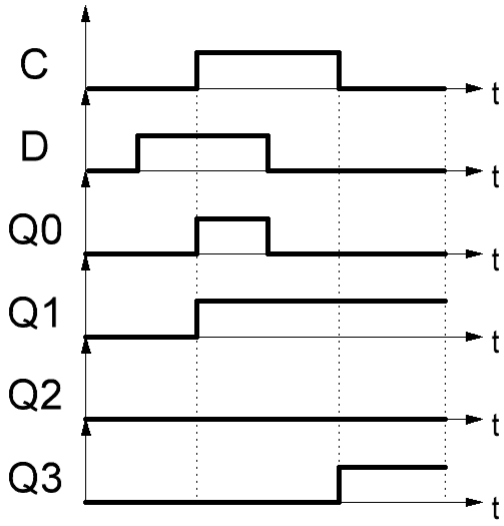

C
Q0 = S0
Q0 = R0
Q0.Q1 = S1
Q0.Q1 = R1
Q0
Q1
t

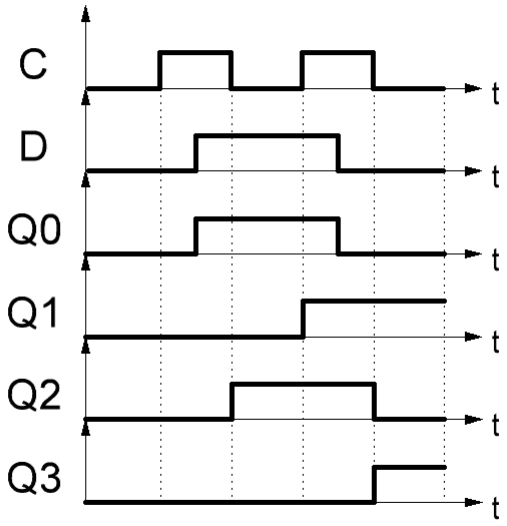

S0
Q0
R0
Q0
C
Q0
Q1
S1
Q1
R1
Q1


C
Q1 = S0
Q0 = R0
Q0.Q1 = S1
Q1 = R1
Q0
Q1
t

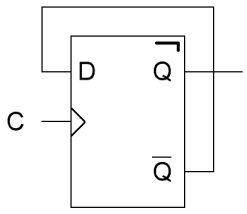
Exercise 2: D Flip-Flops

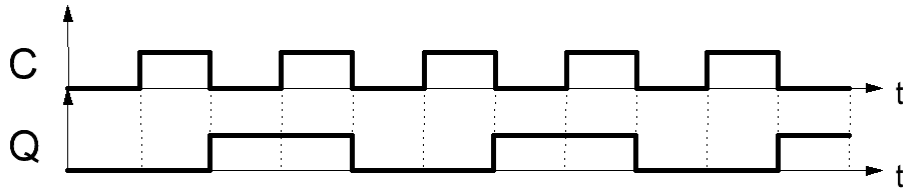
1. Complete the following timing diagrams for a gated D latch (*Q0*), a positive-edge-triggered D flip-flop (*Q1*), a negative-edge-triggered D flip-flop (*Q2*) and a master-slave D flip-flop (*Q3*).

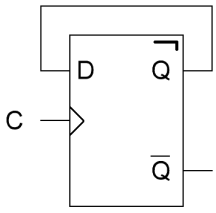


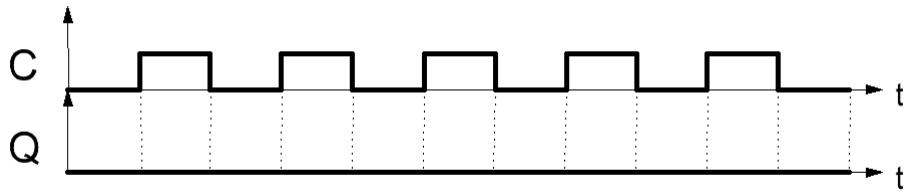


2. Draw the timing diagram of the *Q* output for each of the two circuits below.

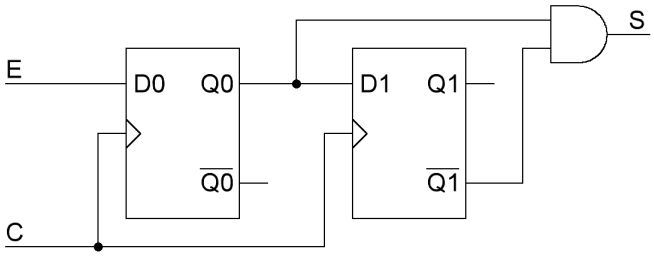


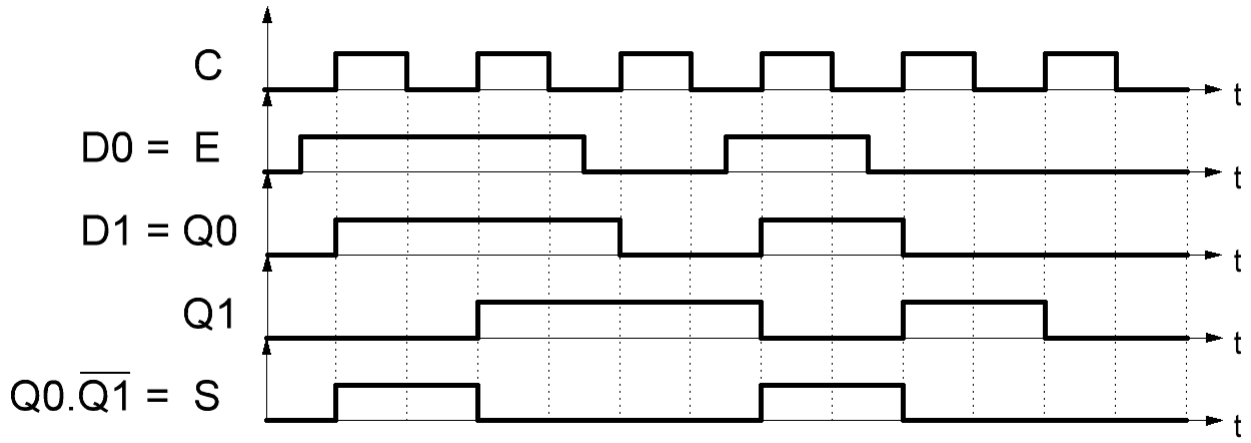




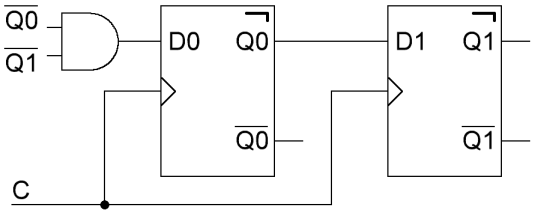


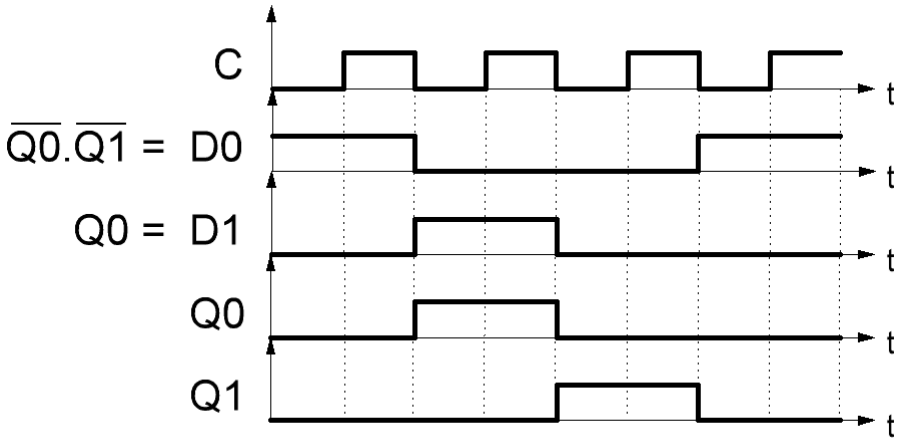
3. Complete the timing diagram for the following circuit.

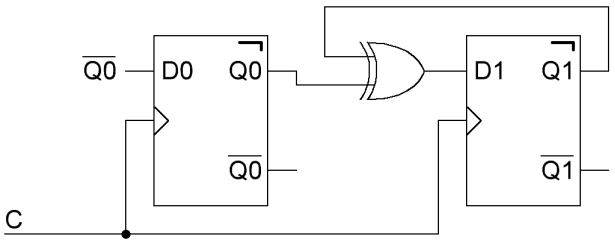


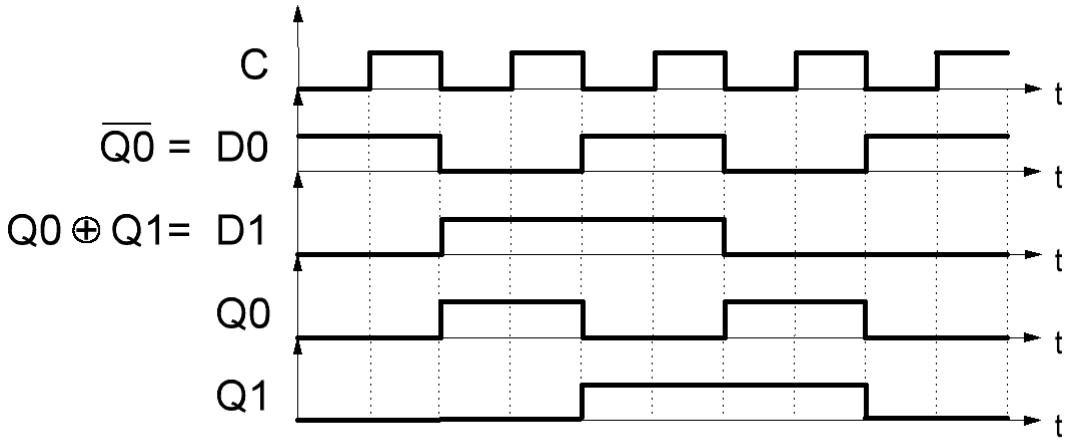


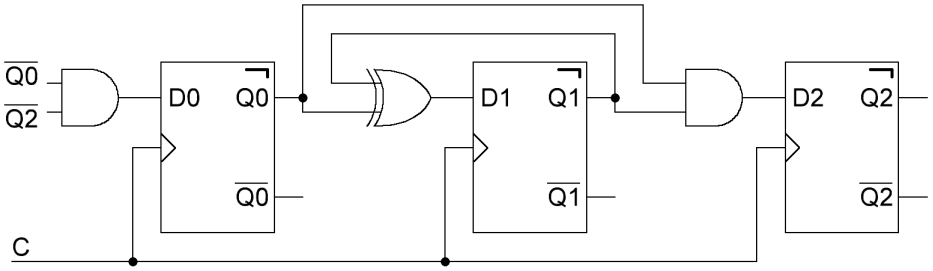
4. Complete the timing diagrams for the circuits below.

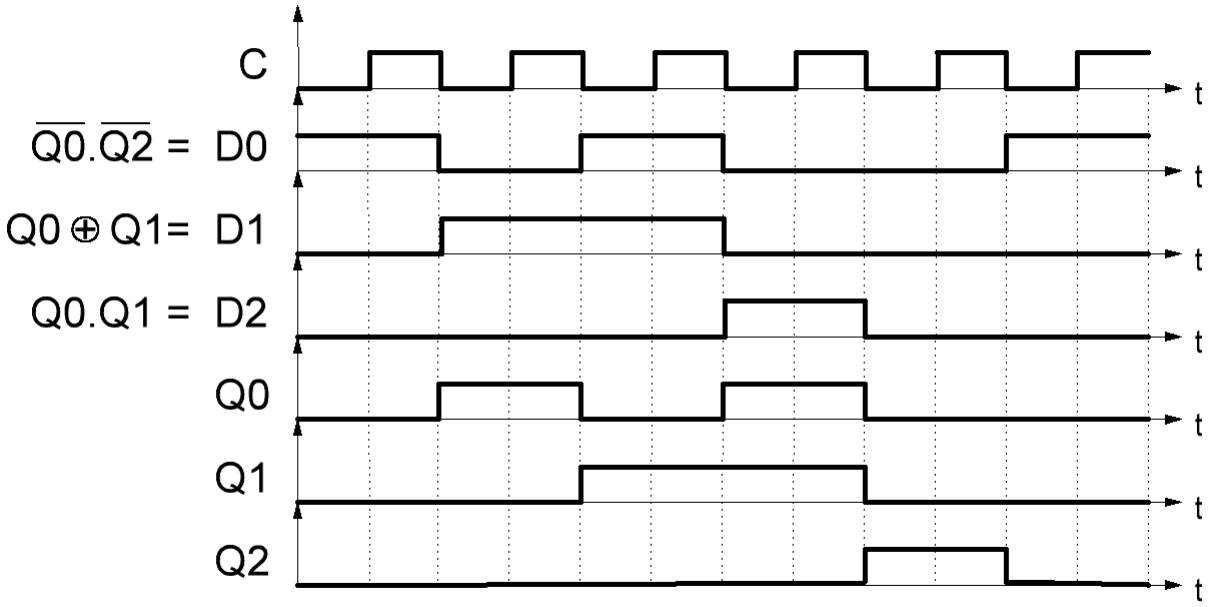





Q0
D0
Q0
Q0
D1
Q1
Q1
C

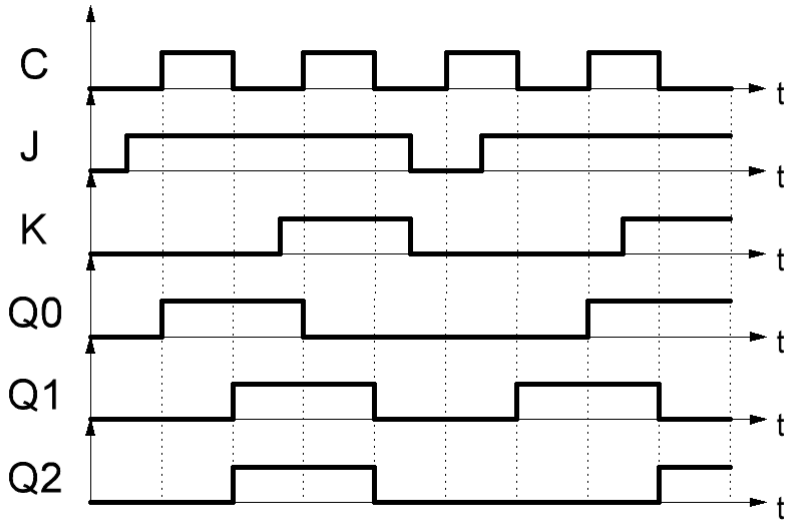

C
Q0 = D0
Q0 ⊕ Q1= D1
Q0
Q1
t


Q0
Q2
D0
Q0
Q0
D1
Q1
Q1
D2
Q2
Q2
C

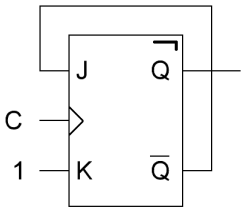

C
Q0.Q2 = D0
Q0 ⊕ Q1= D1
Q0.Q1 = D2
Q0
Q1
Q2
t

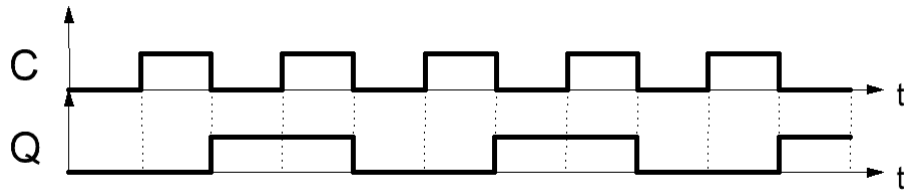
Exercise 3: JK Flip-Flops

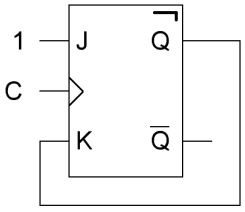
1. Complete the following timing diagrams for a positive-edge-triggered JK flip-flop (*Q0*), a negative-edge-triggered JK flip-flop (*Q1*) and a master-slave JK flip-flop (*Q2*).

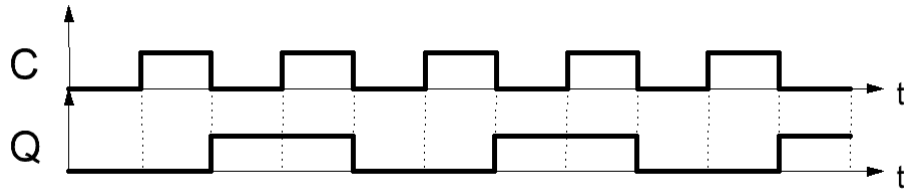


2. Draw the timing diagram of the *Q* output for each of the two circuits below. What is the frequency ratio between *C* and *Q*? What are these circuits called? Find another way to get the same frequency ratio.

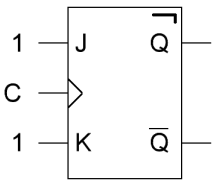




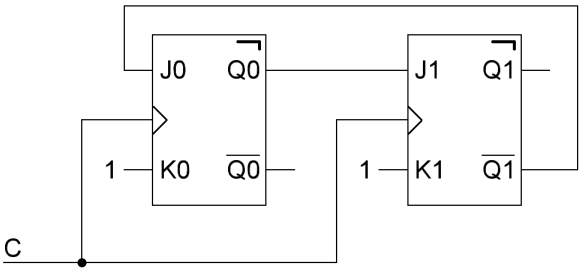


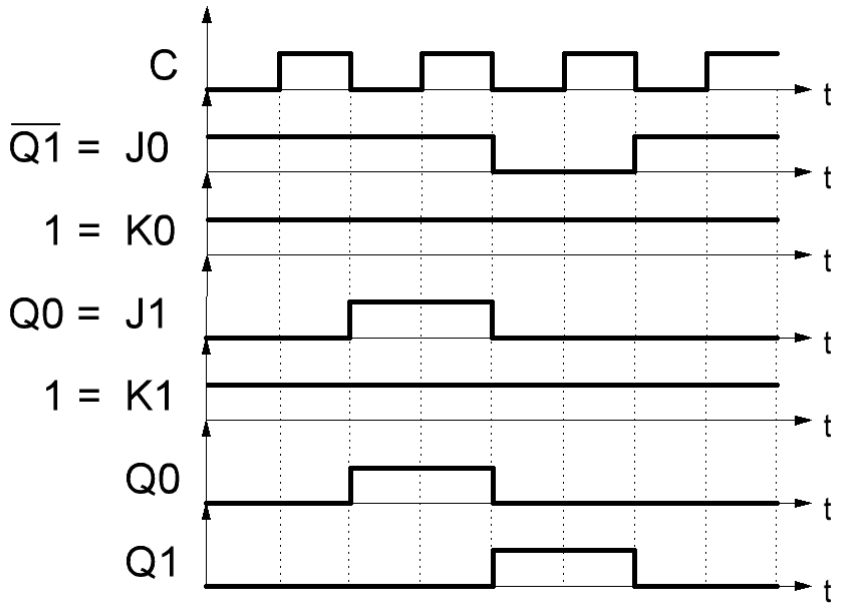


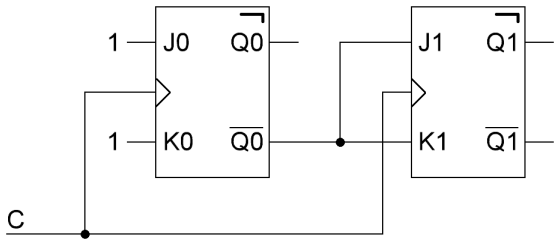
$f_Q/f_C = ½ \rightarrow$ Divide-by-two circuit

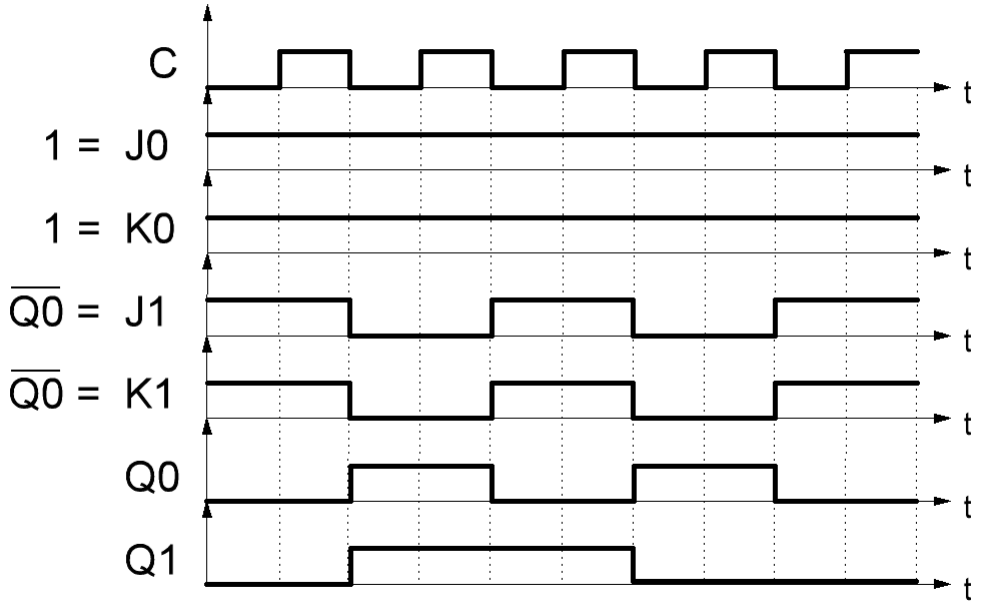


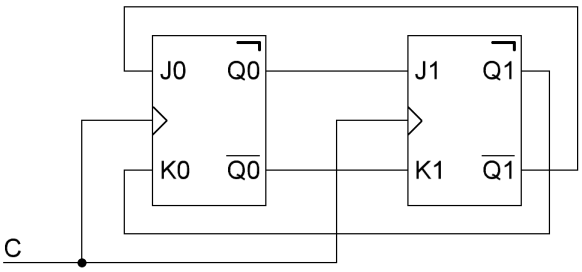
3. Complete the timing diagrams for the circuits below.

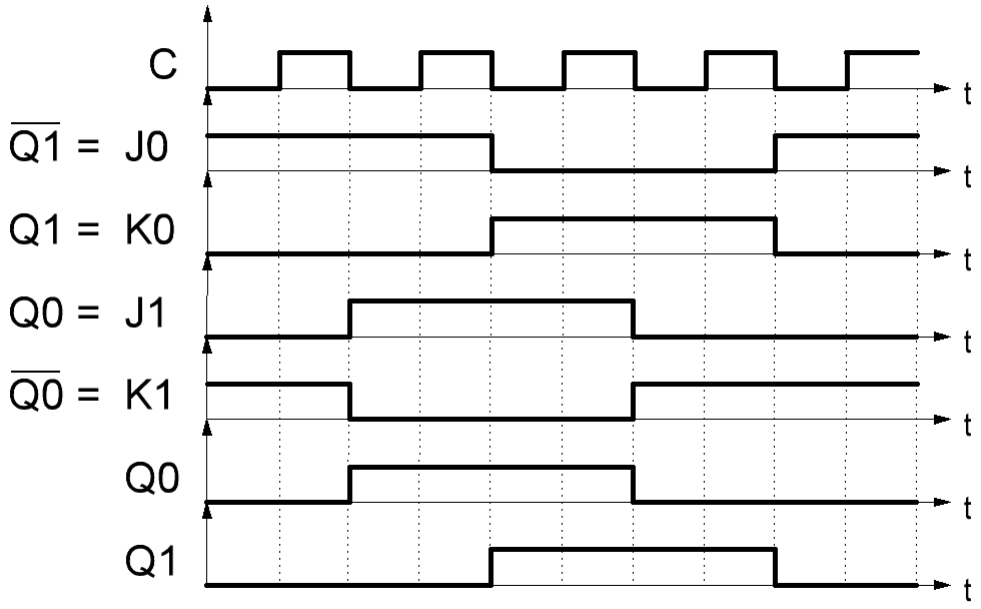




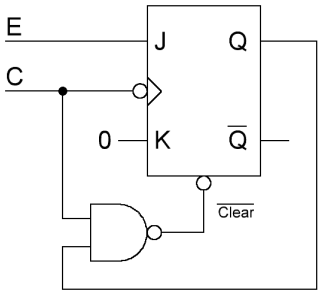


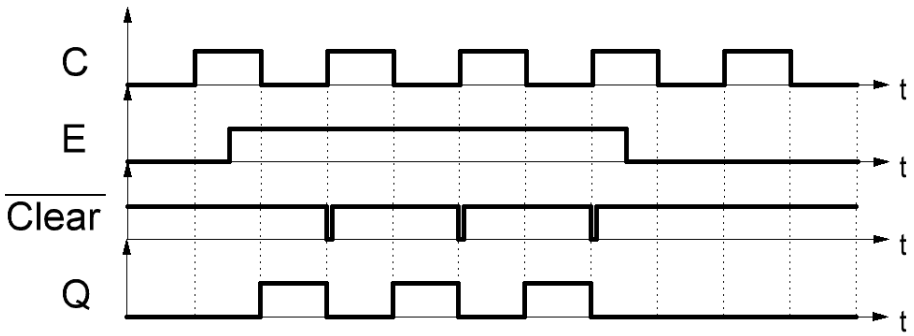






4. Complete the timing diagram for the circuit below.





5. Complete the timing diagram for the circuit below.

